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METHOD FOR FORMING ROBUST SOLDER INTERCONNECT STRUCTURES BY REDUCING EFFECTS OF SEED LAYER UNDERETCHING

Abstract

A method for forming an interconnect structure for a semiconductor device includes defining a via in a passivation layer so as expose a top metal layer in the semiconductor device. A seed layer is formed over the passivation layer, sidewalls of the via, and the top metal layer. A barrier layer is formed over an exposed portion of the seed layer, the exposed portion defined by a first patterned opening. The semiconductor device is annealed so as to cause atoms from the barrier layer to diffuse into the seed layer thereunderneath, wherein the annealing causes diffused regions of the seed layer to have an altered electrical resistivity and electrode potential with respect to undiffused regions of the seed layer.